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655/6000 Core Storage Unit

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N O T E

- a) Whereas the term "655" specifies a combination of defined systems modules resulting in a 6070 system, and because the entire 6000 line consists of system modules fathered by the original 655 specifications, the term "655" is used in a generic sense in this EPS-1 as a matter of convenience.
- b) The High Speed Core Storage Unit is applicable to 6070 and 6080 Systems.
- c) The Low Speed Core Storage Unit is applicable to 6030, 6040, 6050, and 6060 Systems.

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6000/655 CORE STORAGE UNIT

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1.0 GENERAL DESCRIPTION

The 655 Magnetic Core Storage Unit shall be a storage subsystem designed for use as the main store of the 655 Computer. The speed and capacity will be compatible with the high performance of the 655 main frame components. This specification applies to the high speed core storage unit and the low speed (low cost) storage unit. The 655 Core Storage Unit shall be capable of random access and shall contain the core stacks, drive and sense circuitry, power supply, control panels and the necessary logic circuits (including simple self-test features) to permit access from a single 655 System Controller.

The Core Storage Unit shall be capable of performing all storage functions without restrictions on the sequence of addresses accessed, data patterns used or duration of repetitive operations.

The Core Storage Unit will receive data, address and control commands from the system controller and will perform read and write operations. A core controller logic area will generate the necessary timing for storing and retrieving data as well as informing the system controller of illegal actions or fault conditions.

1.1 CORE STORAGE UNIT ORGANIZATION

The Core Storage Unit shall contain a logic section, one or two pairs of 16K x 37 bit storage modules, a local maintenance panel, an operator panel, a power supply panel, and power supplies.
(See Figure 1).

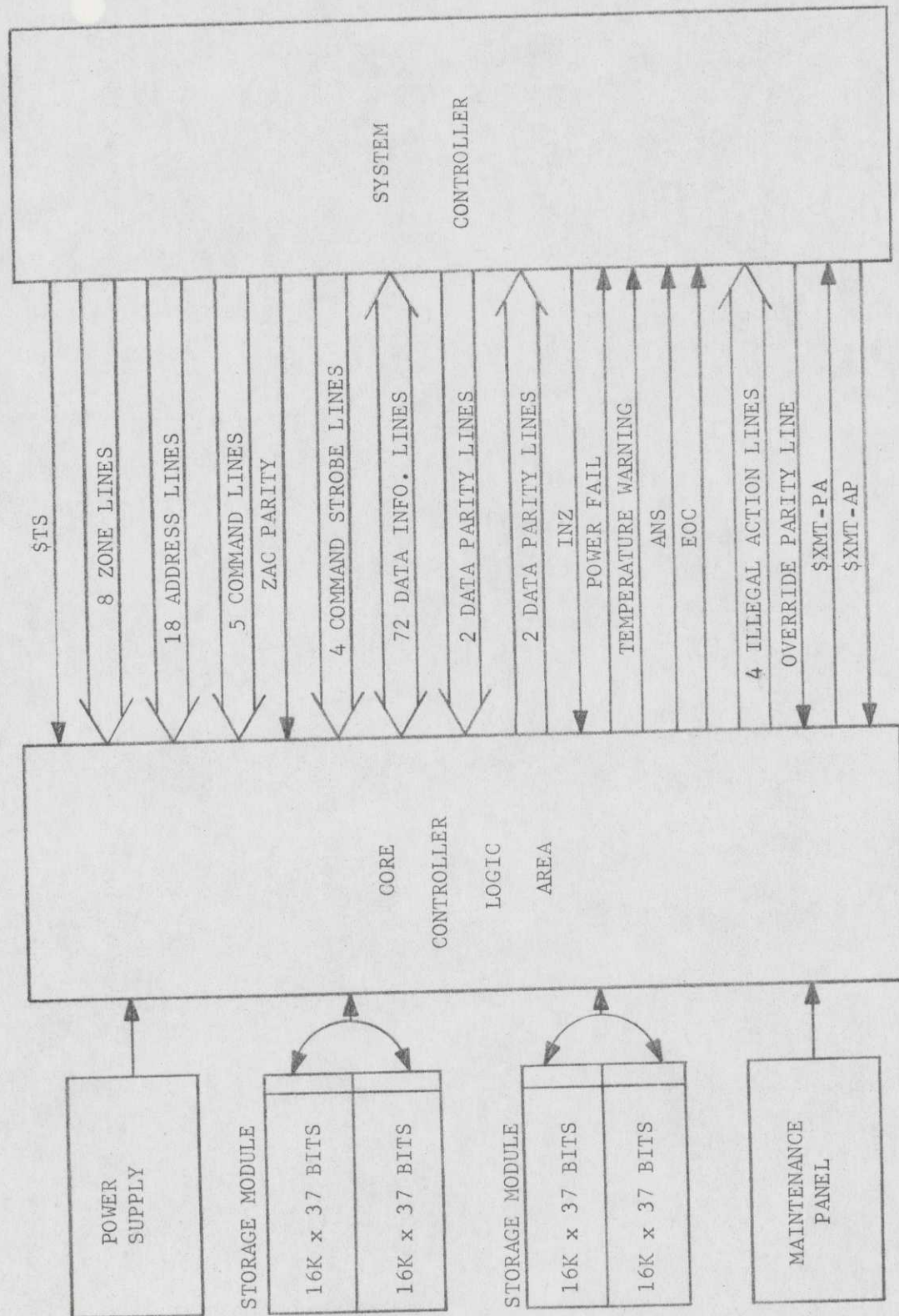


FIGURE 1
CORE STORAGE UNIT ORGANIZATION

1.2 HARDWARE ORGANIZATION

The Core Storage Unit will be housed in a single free-standing cabinet with two-sided access. The cabinet shall either contain a single frame for 32K words x 37 bits, or a dual frame for 64K words x 37 bits. The dual frame shall be separable for shipment. Modules including core planes, drivers, sense amplifiers and address selection circuits will be mounted in the cabinet as single swing out panels. The core control logic area shall be mounted on a single fixed center panel. The Maintenance Panel shall be mounted on a cabinet access panel. All control circuits will be logic circuits common to the 655 processor wherever possible.

1.3 MODULARITY

The core storage unit will be available in modular increments of 32K words x 37 bits. A maximum of two modules will be used per core storage unit.

1.4 TERMINOLOGY AND DEFINITIONS

The following terminology and definitions are used in this specification:

<u>Terminology</u>	<u>Definition</u>
System Controller or "SC"	The controller to which the core storage unit interfaces. This controller is described in EPS-1, #43A219602. (This unit is not described in this specification).
Core Controller Logic Area	That portion of the core storage unit which contains the interface logic, read/write timing, control panel, maintenance panel, and power supply panel.
Core Storage Area (Module)	That portion of the core storage unit containing the magnetic cores, driver circuits, and sense amplifiers.

1.4 TERMINOLOGY AND DEFINITIONS (continued)

<u>Terminology</u>	<u>Definition</u>
Main Store Word	The storage word shall refer to the 72 information bits and two parity bits passed on the storage unit interface. The information bits shall be numbered consecutively from 00 to 71, with bit 00 being the most significant data bit position and bit 71 being the least significant data bit position.
Even Data Word	The even data word shall be bits 00 to 35 of the storage word. Bit PU is to be the parity bit associated with bits 0 to 35. The even word including bit PU shall be located in one stack.
Odd Data Word	The odd data word shall be bits 36 to 71 of the storage word. Bit PL is to be the parity bit associated with bits 36 to 71. The odd word including bit PL shall be located in one stack.
Odd Parity	Odd parity shall mean that the logical value of the parity bit shall be chosen in such a manner that the number of logical "1's" in the word including the parity bit shall be odd.
Abort	A cycle which is aborted must leave the contents of all storage locations unchanged at the end of the cycle. Note that it is <u>not</u> a cycle with an early termination, as parity error information may have to be sent. An aborted cycle is one turned into an RRS type operation which is internal to the storage unit (only).
Zone	A 6- or 3-bit segment of a 36-bit single precision word.

1.4 TERMINOLOGY AND DEFINITIONS (continued)

<u>Terminology</u>	<u>Definition</u>
(AP)	Designates source of signal (System Controller) Active to Passive System Controller to Storage Unit
(PA)	Designates source of signal (Storage Unit) Passive to Active Storage Unit to System Controller
\$	Strobe Pulse, Signal
ZAC (AP)	Zone, Address, Command Bits, 31 lines
D _n (AP) and (PA)	Data Bit n, 72 lines (0-71), bidirectional.
C _n (AP)	Command Bit n, 5 lines (0-4)
A _n (AP)	Address Bit n, 18 lines (0-17)
RRS	Read Restore
CW1	Clear Write by Zone
CW2	Clear Write 72 Bits
RCL	Read and Clear
\$CMD (AP)	Command Strobe Pulse, 4 unique lines (RRS, CW1, CW2 or RCL)
SP	Single Precision (36 bits)
DP	Double Precision (72 bits)
IA _n (PA)	Illegal Action Line n, 4 lines (0-3)
IØI	Inverted on Interface
TØI	True on Interface
'	Complement Line
P _U	Parity Upper
P _L	Parity Lower
\$TS (AP)	Start strobe
\$ANS (PA)	Answer pulse
EOC (PA)	End of Cycle pulse
INZ (AP)	Initialize signal (level)
\$XMIT-AP	Transmit-Write (<u>A</u> ctive to <u>P</u> assive)
\$XMIT-PA	Transmit-Read (<u>P</u> assive to <u>A</u> ctive)

1.5 REFERENCE DOCUMENTS

The following drawing numbers are Honeywell drawing numbers except for those documents controlled on an individual basis. These documents are applicable as they are specified on the date of this specification.

655 Functional Specification	FS68-023
MQX Construction Specification	66A122637
Underwriter's Laboratories Standard	478-1967
MQX Program Data Book	
Core Plane Purchase Specification	66A125835
System EPS-1	43A219600
System Controller EPS-1	43A219602
General Design Requirements for GE-655 and GE-355 Systems EPS-1	43A177851
GE-655 Maintainability, Design EPS	43A219617
MQX Board Tester EPS-1	43A177854

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2.0 FUNCTIONAL CAPABILITIES

2.1 STORE UNIT CAPACITY

The Storage Unit will be available in two sizes: 32,768 x 74-bit Main Store Words and 16,384 x 74-bit Main Store Words. There shall be spare bits provided (see Section 6.1.5) for each word.

2.2 WORD FORMAT

Each Main Store Word of 74 bits shall contain two single precision data words of 36 bits, each with one additional parity bit.

2.3 CYCLE TIME

Cycle time shall be defined as the maximum time required for a full 74-bit Read-Restore cycle as measured at the free end of the store port board connector in the Storage Unit or System Controller.

a) Inherent Maximum Cycle Time:

Inherent cycle time specifies the design speed of the Storage Unit alone; i.e., where cable delays, circuit delays, etc., caused by Central System Modules external to the Storage Unit are assumed to be zero. The Inherent cycle time of the Storage Unit shall be 500 nanoseconds for the high speed storage unit and 1000 nanoseconds for the low speed (low cost) storage unit.

b) Interactive Cycle Time (for reference):

Interactive cycle time specifies the operating speed of the Storage Unit when it is connected to the System Controller. It includes allowances for cable length, circuit variations, margin capabilities, etc., omitted from Inherent cycle time; and therefore reflects the cycle time as seen by the Central System. It is measured at the Store Port Board free edge connector in the System Controller.

The interactive cycle time shall be 530 nanoseconds $\pm$ 30 nanoseconds for the high speed storage unit and 1200 nanoseconds $\pm$ 40 nanoseconds for the low speed (low cost) storage unit; with 10 foot cables. Refer to Note (1) of Figures 2A and 2B.

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2.4 ACCESS TIME

- o High Speed Storage Unit: Data will be available on the output data lines within a nominal 320 nanoseconds (280 ns min., 340 ns max.) from the leading edge of the Start Strobe.
- o Low Speed (low cost) Storage Unit: Data will be available on the output data lines within 1035 nanoseconds max. (300 ns min.) from the leading edge of the Start Strobe.
- o However, the \$ANS Signal from two Storage Units connected to the same System Controller, shall not differ by more than 20 nanoseconds. The Storage Unit shall provide the capability to make this adjustment.

2.5 INSTRUCTION REPERTOIRE

The Storage Unit shall be capable of executing 6 basic instructions: Read-Restore, Read-Clear, Clear-Write 2, Clear-Write by Zone, Read General Register, and Set General Register. An explanation of these operations follows:

2.5.1 Read Restore (RRS) Command

A double precision operation:

- a. During an RRS operation, the Storage Unit will ignore the least significant bit of the address field specified.
- b. The even and odd data words and parity bits (totaling 74 bits), fetched (read) from the storage location specified by the address bits received, shall be made available on the Data lines to the System Controller.*
- c. The parity bits fetched (read) from the storage location, shall be passed on to the system controller unchanged.*
- d. The data words and parity bits at that storage location shall remain unchanged at the end of the storage cycle.*
- e. An Illegal Action (IA/PU/PL), as specified in paragraph 4.4.13, shall be reported by the Storage Unit if a parity error is detected on either (or both) of the fetched (read) even or odd data words.
- f. A parity error detected on the incoming ZAC information lines, shall be reported with an IA code (para. 4.4.13). The incoming parity associated with the data lines and the data lines themselves shall be ignored by the Storage Unit.

*NOTE: Whether or not a parity error is detected on the data fetched (read) from the storage location.

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2.5.1 Read Restore (RRS) Command (continued)

- g. The zone bit field and the command bit field of the ZAC lines are ignored by a RRS command with regard to information content for this command. (But see para. 4.2.0, RGR and SGR commands; these lines are monitored by the Storage Unit.)

2.5.2 Read and Clear (RCL) Command

A single precision operation:

- a. During an RCL operation, for the fetch portion of the cycle only, The Storage Unit shall ignore the least significant bit of the address field received and execute a double precision fetch. However, only one word (36 data bits) is to be operated on.
- b. The even and odd data words and parity bits (totaling 74 bits), fetched (read) from the storage location specified by the address bits received, shall be made available on the Data lines to the System Controller.*
- c. The parity bits fetched (read) from the storage location, shall be passed on to the system controller unchanged.*
- d. If the least significant address bit is a logical "1", bit positions 36 to 71 of the data shall be made logical 0's prior to restoration of the word in core. If the least significant address bit is a logical 0, bit positions 00 to 35 shall be made logical 0's prior to restoration of the word in core. Odd parity shall be stored for the 36 bit word altered by this command.

In both cases, the other word is restored in memory with the original fetched (read) data bits and parity bits unchanged,* as in the RRS cycle.

- e. If a parity error is detected during the fetch (read) cycle, the Storage Unit shall report a parity error (IA/PL/PU) to the System Controller only for the word being operated on, depending on whether the address is odd or even.

*NOTE: Whether or not a parity error is detected on the data fetched (read) from the storage locations.

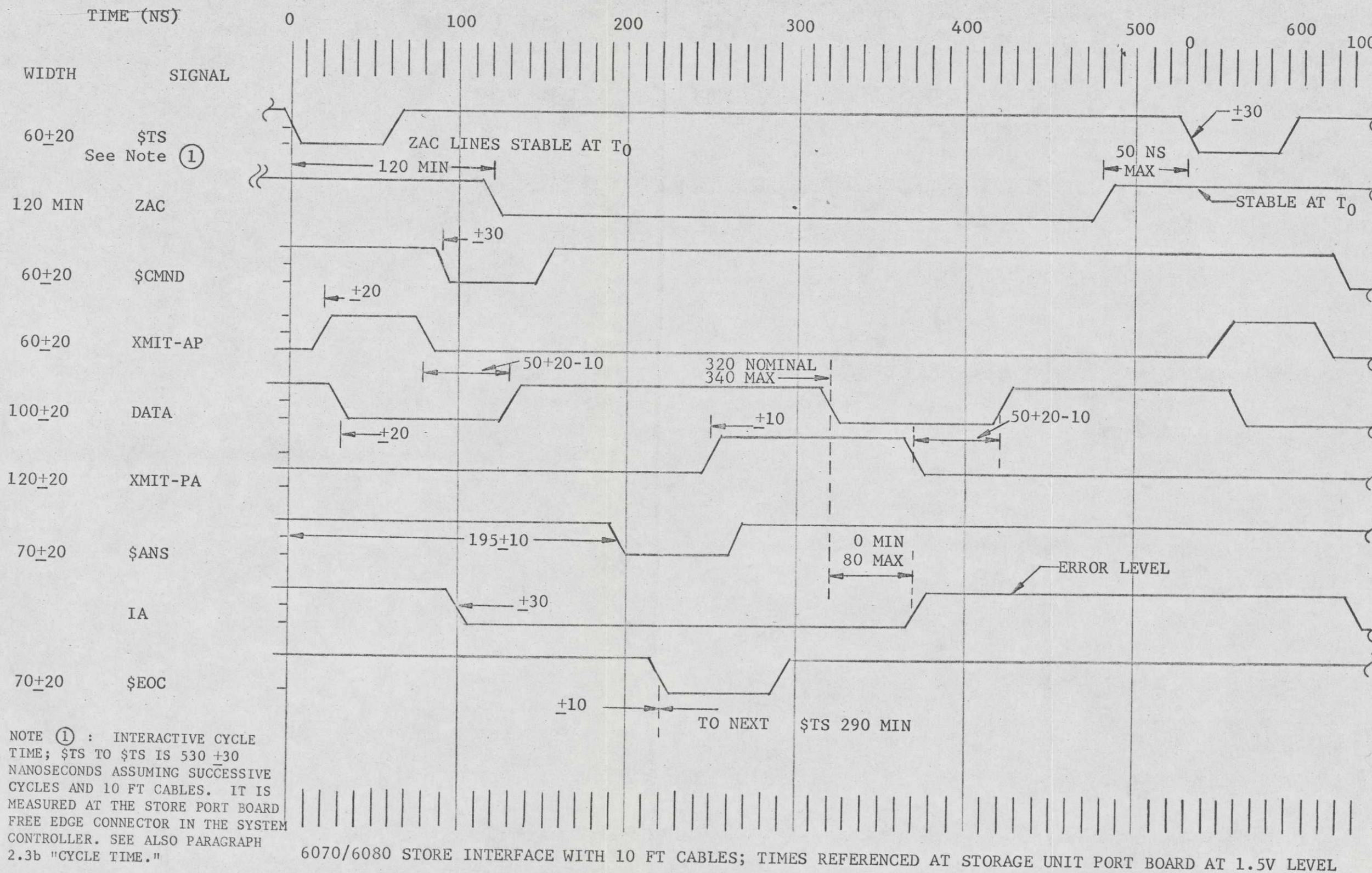
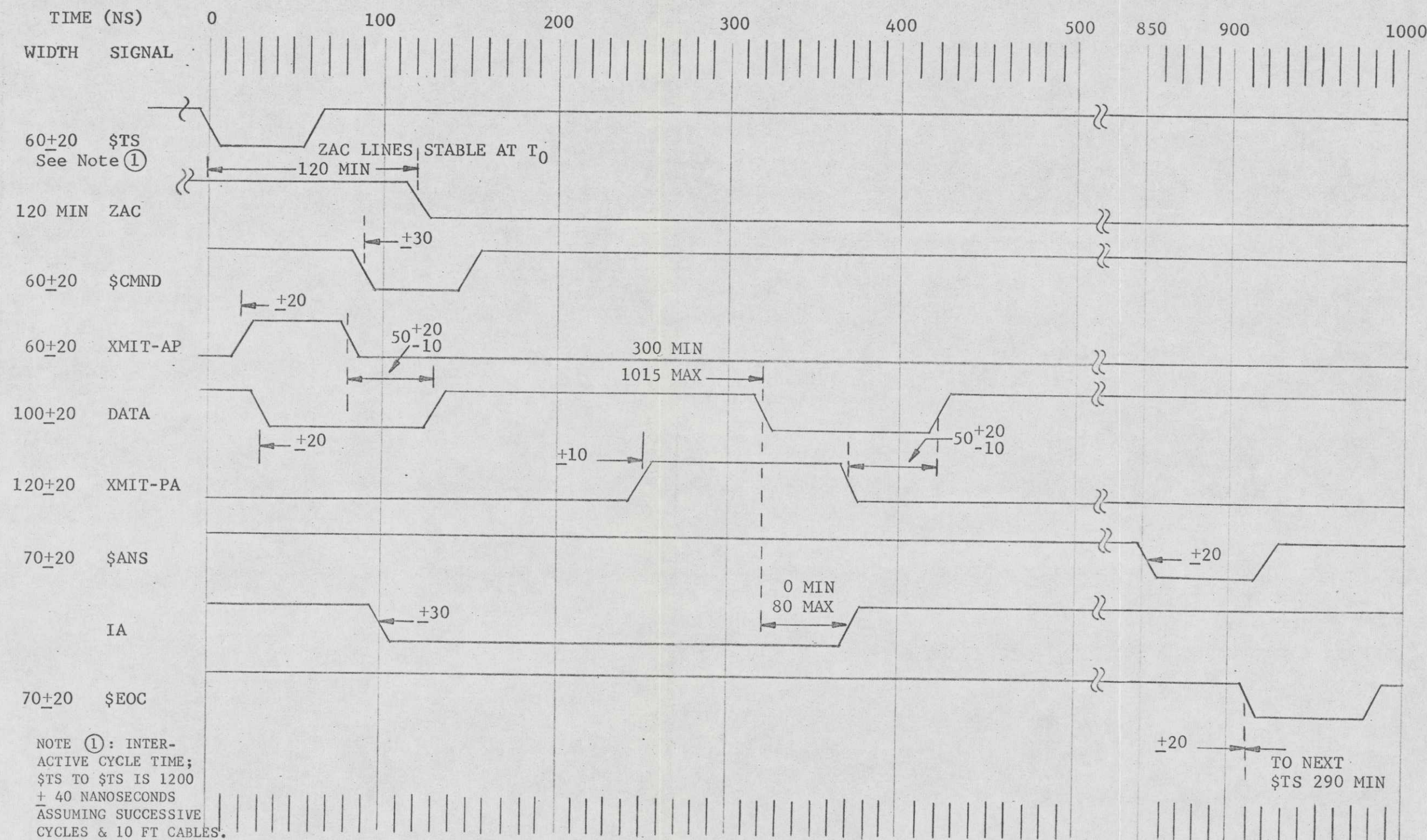


FIGURE 2A



NOTE ①: INTER-
ACTIVE CYCLE TIME;
\$TS TO \$TS IS 1200
 $\pm$ 40 NANOSECONDS
ASSUMING SUCCESSIVE
CYCLES & 10 FT CABLES.

IT IS MEASURED AT 6030-6060 STORE INTERFACE WITH 10 FT CABLES & 6070/6080 MAGNETICS; TIMES REFERENCED AT STORAGE UNIT
THE STORE PORT BOARD PORT BOARD AT 1.5V LEVEL
FREE EDGE CONNECTOR
IN THE SYSTEM CONTROLLER.
SEE ALSO PARAGRAPH 2.3b
"CYCLE TIME."

FIGURE 2B

Despite the parity error, the word being operated on shall be set to zero with correct (odd) parity, and stored in memory as stated in para (d) above. During normal operation, the RCL command shall not be aborted as the result of a parity error detected during the fetch (read) cycle. (See para 2.6.3, Abort Function.)

- f. A parity error detected on the incoming ZAC information lines, shall be reported with an IA code (para 4.4.13) and the command shall be aborted. The incoming parity associated with the data lines, and the data lines themselves shall be ignored by the Storage Unit.

The zone bit field and the command bit field of the ZAC lines are ignored by a RCL command with regard to information content for this command.

2.5.3 CLEAR-WRITE BY ZONE (CW1) COMMAND

A single precision operation:

General Description: This command shall cause specified zones (See Figure 3) of a storage location to be altered while restoring the rest of the word unchanged.

There are two normal variations inherent in this command.

- CW1 - Zone bits are not all logical ones; less than 36 data bits are to be altered in a memory word.
- CW1 - All zone bits are logical ones; all 36 data bits are to be altered (replaced) in a memory word.

*NOTE: Whether or not a parity error is detected on the data fetched (read) from the storage locations.

2.5.3.1 CW1 (Zone bits not all logical ones)

- a. During this CW1 operation, for the fetch portion of the cycle only, the Storage Unit shall ignore the least significant bit of the address field received and execute a double precision fetch. However, only one word (36 data bits) is subject to partial alteration.
- b. The even and odd data words and parity bits (totaling 74 bits), fetched (read) from the storage location specified by the address bits received, shall be made available on the DATA lines to the System Controller. (Note: the System Controller ignores them)
- c. If the least significant address bit is a logical "0", the even word shall be altered (data bit positions 0 to 35) by the CW1 command.

If the least significant address bit is a logical "1", the odd word shall be altered (data bit positions 36 to 71) by the CW1 command.

In both cases, the "other" word is restored in memory with the original fetched (read) data bits and parity bits unchanged,* as in the RRS cycle.

- d. For each field of the specified core location where the corresponding zone line is a logical 1, the contents are replaced with the corresponding bits coming in on the data lines. For each field where the zone bit is a 0, the incoming data is ignored and the original data is restored unaltered. Odd parity shall be generated and stored for the 36-bit data word altered by this command.

EIGHT ZONE LINES	LEAST SIGNIFICANT ADDRESS BIT 17 = 0		LEAST SIGNIFICANT ADDRESS BIT 17 = 1	
	EVEN WORD BITS		ODD WORD BITS	
00	00	- 05	36	- 41
1U	06	- 08	42	- 44
1L	09	- 11	45	- 47
02	12	- 17	48	- 53
03	18	- 23	54	- 59
4U	24	- 26	60	- 62
4L	27	- 29	63	- 65
05	30	- 35	66	- 71

Figure 3 - ZONE ASSIGNMENTS

*NOTE: Whether or not a parity error is detected on the data fetched (read) from the storage locations.

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- e. If a parity error is detected during the fetch (read) cycle, the Storage Unit shall report a parity error (IA/PL/PU) To the System Controller only for the word being operated on, depending on whether the address is odd or even.

Despite the parity error, the word being operated on shall be altered, new correct (odd) parity generated, and stored in memory; as stated in para (c) and (d) above. During normal operation, the CWI command shall not be aborted as the result of a parity error detected during the fetch (read) cycle. (See para 2.6.3, Abort Function.)

- f. The command is aborted if a parity error is detected on the incoming ZAC information or the incoming data word specified by the least significant address bit. Such a parity error will be reported with an IA code as specified in paragraph 4.4.13. The "other" incoming data word shall be ignored by the Storage Unit.
- g. The command bit field of the ZAC lines is ignored by a CWI command with regard to information content for this command.

*NOTE: --whether or not a parity error is detected on the data fetched (read) from the storage locations.

2.5.3.2 CWI (all zone bits are logical ones)

This variation of the CWI command provides the ability to execute a single precision (36 bit) operation. This function is initiated by an active module by sending a CWI command (with all zone bits in the logical One state) to the storage unit. With a few exceptions, it shall function in a manner identical to that specified in para 2.5.3.1.

- a. Same as para 2.5.3.1(a)
- b. " " " " (b)
- c. " " " " (c)
- d. Same as para 2.5.3.1(d) for the condition where all eight zone lines are logical ones.

NOTE: It is desirable, but not mandatory, that the parity bit sent along with the data word (from the System Controller) be written into the addressed memory location directly (bypass the parity generator logic).

- e. The Storage Unit shall not report a parity error which occurs during the fetch (read) cycle; the memory cycle shall not be aborted for this reason.

Despite the parity error, the word being operated on shall be replaced with the data sent from the System Controller and stored in memory; as specified in para (c) and (d) above.

- f. Same as para 2.5.3.1 (f).
- g. Same as para 2.5.3.1 (g).

2.5.3.3 CW1 (all other zone bit combinations);

- a. The Storage Unit shall detect the condition where all eight zone lines are logical zeros. This condition shall be reported with an IA/ZAC parity error even if an actual parity error is not detected. This is a new feature of revision "D"; therefore this is not a requirement of initial storage units.
- b. All other zone bit combinations of logical zeros and logical ones shall be considered valid by the Storage Unit.

2.5.4 Clear Write 72 Bits (CW2) Command

A double precision operation:

This command provides the ability to store a double precision word (data bits 00 through 71) in the storage location specified by the address field received from the System Controller.

- a. During a CW2 operation, the Storage Unit will ignore the least significant bit of the address field received.
- b. The even and odd data words and parity bits (totaling 74 bits), fetched (read) from the storage location, shall be made available on the Data lines to the System Controller. (Note: the System Controller ignores them.)

The storage Unit shall not report a parity error which occurs during the fetch (read) cycle; the memory cycle shall not be aborted for this reason.

- c. The contents of the even and odd storage locations being operated on shall be replaced with the data words and associated parity bits (totaling 74 bits) received from the System Controller.

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2.5.4 Clear Write 72 Bits (CW2) Command (continued)

- d. The command is aborted if a parity error is detected on the incoming ZAC information or the incoming data words. Such a parity error will be reported with an IA code as specified in paragraph 4.4.13.

NOTE: A parity override signal can be used during the CW2 command to store even parity. When this signal is a logical "1", the parity bits sent to the storage unit shall be stored. If the bit is even parity the proper illegal action shall be indicated but the command will not be aborted. If the bit is odd parity it will cause no illegal actions and the command will proceed as normal. (See para. 4.4.14.)

- e. The zone bit field and the command bit field of the ZAC lines are ignored by a CW2 command with regard to information content for this command.

2.5.5 Read General Register Command (RGR)

- a) Paragraph 4.2 specifies the details of the General Register Cycle itself. This command shall cause the contents of the maintenance register (para. 2.6.2) to be returned on data lines 61-71 according to the format specified later in this paragraph.

Bit 71*, returned on the data lines, provides a means for T&D (via the RGR command) to determine if the Mode Register (margins) can be set. This bit is set under the following conditions:

The Test/Normal" switch is in the "Test" position; and the power supply Remote/Local switch is in the "Remote" position.

OR

The System Control Center (SCAM) places the Storage Unit in the "Test" state; and the power supply Remote/Local switch is in the "Remote" position.

*See note at end of this paragraph (a).

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2.5.5 Read General Register Command (RGR) (continued)

<u>*Data Bit</u>	<u>Function</u>
0-35	All zeros
PU	Odd Parity Bit
36-60	Zeros
61	+5 Volt Margin Bit 1
62	+5 Volt Margin Bit 2
63	Bit Voltage Margin Bit 1
64	Bit Voltage Margin Bit 2
65	Word Voltage Margin Bit 1
66	Word Voltage Margin Bit 2
High Speed { 67	Zero
Store Only { 68	\$ Sense Amp. Margin Bit 1
	\$ Sense Amp. Margin Bit 2
Low Speed/ { 67	\$ Sense Amp. Margin Bit 1
Low Cost { 68	\$ Sense Amp. Margin Bit 2
Store Only { 69	\$ Sense Amp. Margin Bit 3
70	Zero
71	{ If "0", Store Unit in "Normal" state. If 1, Store Unit in "Test" state.
PL	Odd parity bit.

*NOTE(a): In the initial models these items are not implemented in their entirety. See Project Plan for implementation schedule.

b) Margin Bit Functions:

- o Voltage Margins; High Speed and Low Speed/Low Cost Storage Units:

<u>Bit 1</u>	<u>Bit 2</u>	<u>For Voltage</u>
0	0	Normal
0	1	-5%
1	0	+5%
1	1	Illegal, results unpredictable.

- o Timing Margin Functions; High Speed Storage Unit only:

<u>Bit 1</u>	<u>Bit 2</u>	<u>\$ Sense Timing</u>
0	0	Normal
0	1	Slow (late)
1	0	No strobes
1	1	Fast (early)

2.5.5 Read General Register Command (RGR) (continued)

- o Timing Margin Functions; Low Speed/Low Cost Storage Units only:

<u>Bit 1</u>	<u>Bit 2</u>	<u>Bit 3</u>	<u>\$ Sense Timing</u>
0	0	0	Nominal
1	0	0	+ 5 ns. late from nominal.*
0	1	0	+10 ns. late from nominal.
1	1	0	+15 ns. late from nominal.
0	0	1	+20 ns. late from nominal.
1	0	1	-15 ns. early from nominal.
0	1	1	-10 ns. early from nominal.
1	1	1	- 5 ns. early from nominal.

*NOTE: The values assigned by this EPS-1 are subject to change. They are included for clarification of intent only. The EPS-2 will contain the actual values assigned.

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- c. A total of 74 bits (including the two odd parity bits) shall be made available on the Data Lines to the System Controller.
- d. Refer to paragraphs 2.6.2 (Maintenance Register), 3.2.1 (Normal/Test Switch), and 4.2 (General Register Cycles) for further details.
- e. The RGR command shall be accepted by the Storage Unit in both "Normal" and "Test" on-line operation.

2.5.6 SET GENERAL REGISTER COMMAND (SGR)

This command shall cause the contents of data lines 61-69 to set the maintenance register. The format of the maintenance register is shown in Section 2.5.5.

Refer to paragraphs 2.6.2 (Maintenance Register), 3.2.1 (Normal Test Switch), and 4.2 (General Register Cycles) for further details.

- 2.5.7 LEGITIMATE MARGIN COMBINATIONS The SGR command shall not be accepted by the Storage Unit unless the Storage Unit is in Test Mode and On-Line, or the System Control Console (SCAM) places the unit in "Test". (see para. 3.2.1.2).

The Storage Unit shall be designed to function within timing specifications and tolerances only with the following margin bit combinations:

SYSTEM CONTROLLER		STORAGE UNIT	
\$TS	Offset	\$Sense	Power Supply Margins
Fast	NO	Normal	Normal
Slow	Yes	Normal	Normal
Normal	Yes	Normal	Normal
Normal	No	Normal	Margin bit 1 or 2, all voltage combinations
Normal	No	Any of the legal timing margins	Normal

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The general rule to follow can be summarized as follows:
When margin conditions are set in one System Module (such as the Storage Unit) the connecting System Module shall be in the normal state (no margin conditions set). Within a given System Module, voltage margin conditions and timing margin conditions shall not be set simultaneously.

2.6 SPECIAL FEATURES

2.6.1 STORAGE PROTECTION

The storage unit shall have provision for terminating and resuming normal memory operation without loss of data in the event of any interruption of primary power.

2.6.2 MAINTENANCE REGISTER

There shall be a register provided to store the functional state of certain internal signals and voltage supplies (see para. 2.5.5). The contents of this register can be retrieved with an RGR command. The functions reflected by the contents of this register are set (enabled) with an SGR command (see para 2.5.6). Note that the power supply "Remote/Local" margin switch must be in the "Remote" position to enable the Maintenance Register.

The Maintenance Register (and the functions represented by its contents) shall be reset to the zero state (normal state) when the Normal/Test switch is in the Normal position and the 655 Systems Control Center reflects the "margin override" (normal) state, or when the Storage Unit is initialized, or by an SGR command (bits 61-69 set to zero).

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2.6.3 ABORT FUNCTION

The Storage Unit shall provide the abort function defined in para. 1.4, Terminology and Definitions, for the RCL and CW1 (zone bits not all logical ones) commands, as a maintenance aid.

Normally the abort logic shall be in the disabled state; i.e., the RCL and CW1 function as specified in para. 2.5.2 and 2.5.3.1. The abort function shall be enabled by a switch or jumper wire, and shall be designed for on-line operation. If a switch is used, the function shall be enabled when the "Test/Normal" switch is in the "Test" position.

When enabled, the command shall be aborted if a parity error is present during the fetch (read) cycle; the cycle shall be aborted for the 36 bit data word being operated on only. In all other ways, the RCL and CW1 shall function as specified in para. 2.5.2 and 2.5.3.1.

During the Test and QC phases of manufacturing, this feature should prove to be useful because unproven memories are being dealt with. The logic may also be useful to field personnel when store problems of a particularly evasive nature are encountered, which do not yield to all the other maintainability features provided by the system.

For reference only: When enabled, the Interactive Memory Cycle Time (para. 2.3), for the CW1 (zone bits not all ones) and RCL commands only, will be increased to 600 nanoseconds.

3.0 CUSTOMER INTERFACE REQUIREMENTS

The following control panels are provided in the core storage unit.

3.1 OPERATORS PANEL

A standard 655 operators panel shall be mounted on the outside of the cabinet access door to provide standard cabinet control and indication. The following switches and indicators shall be located on this panel.

3.1.1 AC BREAKER ON INDICATOR

An indicator shall be provided that shall be lit whenever the circuit breaker for the Core Storage Unit is closed.

3.1.2 POWER ON SWITCH/INDICATOR

A momentary pushbutton/indicator shall be provided that will turn on main power to the cabinet when depressed and that shall be lit while the main power is on.

3.1.3 POWER OFF SWITCH/INDICATOR

A momentary pushbutton/indicator shall be provided that will turn off main power to the cabinet when depressed and that shall be lit while the main power is off.

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3.1.4 NORMAL/TEST INDICATOR

This split field indicator reflects the status of the Normal/Test switch (see para 3.2.1).

<u>Switch Position</u>	<u>Indicator State</u>
Normal (On-line)	"Normal" field illuminated
Test	"Test" field illuminated
Off-Line	"Test" field illuminated

3.1.5 Ready/Trouble Indicator

This split field indicator reflects whether the Storage Unit is "Ready"; in an On-Line (Normal or Test) operational state, or in a "Trouble" state (a condition exists which prevents the Storage Unit from being used in the System). Out of tolerance temperature or voltage conditions, Off-Line state, blown fuses, stop on fault condition set and failure detected, or other disabling failure, are examples of the type of conditions which cause the "Trouble" field to be illuminated.

3.1.6 Overtemperature Indicator

This indicator shall be lit by the overtemperature sensors as a warning that the Core Storage Unit is running at above normal temperature. At this time, the light shall be lit and a local audible alarm shall be turned on.

3.1.7 Alarm Reset Switch/Indicator

A momentary pushbutton/indicator shall be provided to both indicate that the local audible alarm has been set and to allow resetting of this alarm.

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3.2 MAINTENANCE CONTROL PANEL

A maintenance control capability shall be implemented to provide a local control and indicator facility for off-line testing of the storage unit. The following switch and indicator functions shall be provided.

3.2.1 Normal/Test Switch

3.2.1.1 a) On-Line/Test/Off-Line* Switch (Initial Storage Units):

A three position switch is provided to indicate to the Storage Unit whether it shall be controlled by the Maintenance Panel or by external System Modules, and whether the contents of the Maintenance Register can be changed (or read) by a General Register command. When the switch is in the "Normal" (On-Line) position, maintenance panel switch functions shall be disabled.

b) Initial Storage Units:

Initial models of the Storage Unit functionally behave in accordance with the following chart (Table 3.2.1.1); note that both the On-Line/Test/Off-line switch and the Data Display switch interact.

*NOTE: See footnote paragraph 2.5.5(a).

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3.2.1.1 (continued)

Data Display Switch; Para 3.2.2 Normal/Test Switch; Para 3.2.1	Data Display	Port Display	Test
On-Line	RGR & SGR Disabled	RGR & SGR Disabled	RGR & SGR Disabled
Test	SGR-OK RGR-NO	SGR-OK RGR-NO	SGR-OK RGR-OK
Off-Line (Maintenance Panel Control)	N	D	T

Note:
T&D margin checks require both switches to be in the Test position.

Where:

N = Normal on-line or off-line position.
 D = Display only - not cycling
 T = For timing checks (with oscilloscope) - no error detection.
 RGR = Read General Register Command
 SGR = Set General Register Command

Note 1: When the On-Line/Test/Off-Line switch is returned to the On-Line position, the Maintenance Register is reset (cleared to zero) and all margin conditions are returned to the Normal state.

Table 3.2.1.1

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3.2.1.1 (continued)

Note 2: Off-Line; effect on System Controller Interface:

- Signals received from the System Controller are ignored.
- Signals presented on the cable to the System Controller are at their high voltage level (DC level).

Note 3: Initial Storage Units do not have SCAM related functions implemented in their entirety.

3.2.1.2 Subsequent Storage Unit Models

In order to be consistent with initial Storage Units, the three position "Normal/Test" switch described in the previous paragraph (3.2.1.1a) shall be implemented. However, the System Control Console (SCAM logic) shall be provided with the ability to place the Storage Unit in an on-line "Test" state when the "Test/Normal" switch is in the "Normal (On-Line)" position.

Test/Normal Switch

This three-position switch provides a local means to indicate to the Storage Unit and System Controller whether or not Maintenance features of the Storage Unit shall be enabled or disabled. When in the "Normal" position, these maintenance features shall be disabled.

- When in the Test position, the Storage Unit shall be in an on-line state and the appropriate on-line maintenance features shall be manipulated under program control (e.g., margins).
- When in the "Off-Line (Manual)" position, the Storage Unit shall be placed in an off-line state to the System Controller (the balance of the Central System). The balance of those Maintenance panel functions appropriate to off-line testing and maintenance shall be enabled.

Note: The System Control Console SCAM capability is a 6000 Line system option offered to each customer. The design of subsequent Storage Unit Models must anticipate that some customers will request this feature. Therefore, those functions necessary for properly interfacing and responding to the optional installation of SCAM modules shall be provided by these subsequent models.

3.2.1.2 Subsequent Storage Unit Models (continued)

- a) The following briefly describes the functional interaction of the Normal/Test switch, the System Control Console (SCAM), and Normal operation.

Normal on-line operation, normal error detection.	On-line operation, all programmable maintenance aids.	Off-Line, Manual aids.
SU Normal state and SCC Normal state.	SU Test state. OR SU "Normal" and SCC dictates Test State.	SU Off-Line (Manual) state.

Where:

SU means Storage Unit.

SCC means System Control Console.

- b) The following table (3.2.1.2) describes the functional behavior of SCAM and this switch. Note that the "Data Display" switch no longer interacts with the Test/Normal function, but the power supply "Remote/Local" switch does (para.2.6.2).

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Normal/Test Switch	SCAM Normal/Test	
Case ① Normal (On-Line)	Normal	• Maintenance Panel functions disabled. • On-Line RGR commands executed. • On-Line SGR commands converted to RRS to Memory. • On-Line Interface to the System Controller. • SCAM can enable/disable on-line programmable maintenance aids from the System Control Center; also SCAM logic can turn power on and off, initialize, and monitor the SCAM status lines.
Case ② Test	Normal (No Effect)	• Both SGR (margins) and RGR commands executed. • On-Line Interface to the System Controller. • SCAM cannot enable/disable on-line programmable maintenance aids. • SCAM can turn power on and off, and monitor the SCAM status lines.
Case ③ Off-Line	Normal (No Effect)	• Off-Line maintenance panel features enabled. • Off-Line interface to System Controller. • SCAM cannot enable/disable on-line programmable maintenance aids. • SCAM can turn power on and off, and monitor the SCAM status lines.
Case ④ Normal	Test	• Same as case ② except: • Programmable maintenance aids are enabled by SCAM (margins).
Case ⑤ Test	Test (No Effect)	• Same as Case ② .

Table 3.2.1.2

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3.2.1.2 Subsequent Storage Unit Models (continued)

- c) When the "Test/Normal" switch is returned to the "normal" position, the Maintenance Register shall be reset (cleared to zero) and all margin conditions returned to the Normal state (except if SCAM is enabling margin conditions).
- d) Conversely, if the SCAM "enable/disable margins" line returns to the Normal state, the Maintenance Register shall be reset (cleared) and all margin conditions returned to the Normal state (provided the "Test/Normal" switch is already in the "Normal" position).
- e) Off-Line; effect on System interfaces
 - System Controller Interface:
 - Signals received from the System Controller shall be ignored.
 - Signals sent out on the cable to the System Controller shall be at their high voltage level (DC level).
 - SCAM Lines:
 - The SCAM logic of the System Control Console can still turn power on and off, and monitor the SCAM lines. By monitoring the SCAM "Normal/Test" line and "Ready/Trouble" line (among others), appropriate indicators on the System Control Console will be illuminated to define the state of the Storage Unit.

3.2.2 DATA SWITCHES

Thirty-six (36) data switches shall be provided for manually entering information into the storage unit, excluding parity (generated by the parity logic in the storage unit). Data bits may also be specified by selecting a bit pattern as described in Section 3.2.3. Data switches shall also be affected by the True-Complement Switch (see Section 3.2.4). Note that the same pattern is set for bits 0-35 and bits 36-72.

3.2.3 PATTERN SELECT SWITCHES

Switches shall be provided to select the pattern to be used for the data bits of storage unit cycles. The patterns shall include but are not limited to: worst case patterns, all ones, all zeros, bit complement, address storage and parity bit worst case. If no pattern select switch is on; the data bits shall be set from the Data Switches.

3.2.4 TRUE-COMPLEMENT SWITCH

A switch shall be provided to control the state of the pattern selected by the Pattern Select Switches.

3.2.5 DATA LIGHTS

Indicator lights shall be provided to display the 72 information bits and 2 parity bits in a storage location.

3.2.6 INT/EXT CLOCK SWITCH

A switch shall be provided to select the internal clock or allow an external clock to control the core controller signals. The external clock is connected through a connector provided on the maintenance panel.

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3.2.7 ADDRESS COUNTER

A counter shall be provided to increment the number formed by all the Address Switches set to "count" (see Section 3.2.8). The Address Counter shall be set to zero by the Initialize Switch, and shall increment with each memory cycle.

3.2.8 ADDRESS SWITCHES

There shall be 16 3-position address switches provided to select the 16 bits of the address to be used for storage unit cycles. Each of the 16 switches may specify its bit position to be a "1", a "0", or "count" (the same as the corresponding bit of the address counter).

3.2.9 ADDRESS LIGHTS

There shall be 16 lights provided to display the contents of the storage unit address register.

3.2.10 COMMAND SWITCHES

Command switches shall be provided for manually selecting storage unit commands of RRS and CW1.

3.2.11 COMMAND LIGHTS

Lights shall be provided to display the contents of the command register.

3.2.12 ZONES

Provisions shall be made such that when the storage unit is "Off-Line," all zone bits will be forced to a logic "1."

3.2.13 START PUSHBUTTON

There shall be a start pushbutton switch to initiate maintenance panel operations with the storage unit.

3.2.14 STOP PUSHBUTTON

There shall be a stop pushbutton switch to halt maintenance panel operations when the storage unit is in a continuous mode of operation (see Section 3.2.15).

3.2.15 SINGLE STEP/CYCLE RATE SWITCH

A switch shall be provided to select two modes of operation. One mode is "Single Step," whereby only one storage unit cycle is executed each time the "Start" pushbutton is depressed. The other mode is "Cycle Rate," whereby Storage Unit cycles are continually executed at the selected rate. Operation is initiated by depressing the "Start" pushbutton, and operation is terminated by depressing the "Stop" pushbutton.

3.2.16 STOP ON ERROR/NOT STOP ON ERROR SWITCH

A switch shall be provided to select or not select storage unit cycles to stop on a compare error and/or a parity error. A compare error occurs as follows. When a read command is executed from the maintenance panel, the fetched word shall be compared with the word that was supposed to have been stored in that memory location. The Data Switches or a Pattern Select Switch (if one is set) shall indicate what pattern should have been stored in core. If the fetched word does not compare with the word that should have been stored, a compare error shall be indicated.

Note: But see para 3.2.22, Data Display switch.

3.2.17 ERROR LIGHT

A light shall be provided to indicate that a parity or compare error has occurred.

Note: But see para 3.2.22, Data Display switch.

3.2.18 INITIALIZE SWITCH

There shall be an initialize switch to send an initialize signal manually to the storage unit (para 4.4.8) only.

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3.2.19 SPEED CONTROL

A speed control shall be provided so that the speed of the maintenance tester can be varied from .450 usec to 2.5 usec (approximately).

3.2.20 32K-64K SWITCH

A switch shall be provided to indicate to the storage unit logic the size of the storage modules available (32K or 64K).

3.2.21 LAMP TEST

A means will be provided for testing of all indicator lamps.

3.2.22 DATA DISPLAY SWITCH

Switch Position	Function Displayed
Port Display	Port Board Register
Data Display	Memory Register (when "off-line," this switch must be in "Data Display" position for error detection; initial storage units).
Test	Enable Maintenance Register and functions, (initial storage units).

3.2.23 OTHER LIGHTS AND SWITCHES

In addition to those specified, other lights or switches may be provided as necessary to diagnose storage unit failures.

3.3 POWER SUPPLY CONTROL PANEL*

The power supply control panel will contain switches to turn power on and off. This control panel, located on the power supply, will also contain indicator lamps for presenting the status and high/low volt margin switches.

* (See footnote, para 2.5.5).

3.3.1 POWER ON INDICATORS

For each regulator, when D.C. power is on, an indicator will be illuminated yellow. When power is off, this indicator will not be illuminated.

3.3.2 POWER FAILURE INDICATORS

For each regulator, in the event of a D.C. power failure or an out of tolerance condition, an indicator will be illuminated red and latched in that state. Once latched, the indicator shall require manual intervention to turn it off.

3.3.3 OVER/UNDER VOLTAGE OR CURRENT SIGNAL

The Storage Unit power supply shall indicate when the D.C. power supply voltage or current is out of legal tolerance. The Storage Unit shall send this signal to the System Controller.

3.3.4 ELAPSED POWER ON TIME METER

A meter shall be provided to indicate the cumulative time that secondary power has been applied to the storage unit. Meter shall record up to 99999.9 hours.

3.3.5 Voltage Potentiometer

A manual potentiometer shall be provided to allow the power supply to be varied so the output voltage can cover the range set by the Schmoo Diagram. This potentiometer can be adjusted when the core storage unit is in the on-line mode (see Section 3.2.1).

4.0

HARDWARE INTERFACE

There shall be two major types of interface lines:

- a) Data Lines - The 72 information bits shall be transferred over 72 bi-directional lines. The two data parity bits shall be transferred over 4 uni-directional lines, 2 going to the Storage Unit, 2 coming from the Storage Unit.
- b) Control Lines - There shall be 49 uni-directional control lines passing control information between the Core Controller and the System Controller. These lines are shown in Figure 1.

There shall be two major types of cycles: store and general register. The store cycles shall be concerned with reading and writing core storage. The general register cycles shall be concerned with reading and writing into the general register located in the storage unit.

4.1

STORE CYCLES

The Zone, Address, and Command lines (ZAC), together with the Start Strobe (\$TS) and Command Strobe lines (\$CMD), shall contain the control information necessary to execute the store cycles RRS, RCL, CW1, and CW2.

For all interface timing relationships and specifications refer to figures 2 and 4.

Within the Storage Unit, all the store cycles perform a double precision fetch (read) operation, which is then followed by either a restore, full write, or partial write operation (depending on the command/strobe received). Conceptually, each store cycle is initiated by the \$TS signal. Note that successive \$TS signals have a definite relationship to memory cycle time in terms of the store port interface, and therefore shall not occur more frequently than specified in figures 2 and 4. At \$TS time, the ZAC lines contain valid address information for use by the forthcoming store cycle. Upon receipt of the \$TS pulse from the System Controller, the Storage Unit processes the address field (lines), initiates the fetch (read) portion of the store cycle common to all commands, and begins to check parity on all the ZAC information (lines). At a specific time after \$TS, the command strobe (\$RRS, \$RCL, \$CW1, \$CW2) is received by the Storage Unit; if not received in time, a time-out failure is reported (IA/command strobe failure) and the store cycle is

aborted. In addition, the Storage Unit determines whether ZAC parity and data parity (CW1 and CW2 only) are correct; if not, the store cycle is aborted. If parity is correct, subsequent store cycle actions depend on the command (strobe) received (RRS, RCL, CW1, CW2). Each of these are specified in detail in Section 2.5.

Note that five command bits are transmitted to the storage unit and are involved only in the parity check (except; see General Reg. Cycles, para 4.2). These command bits will not be used to specify the command to be executed. Command information will be sent on the command strobe lines (\$CMD).

At the end of each storage unit operation, all logic registers shall contain information pertaining to that operation as an aid to maintenance. The information shall be retained until the initiation of the next storage unit operation, or until the storage unit receives an initialize signal.

4.2

GENERAL REGISTER CYCLES

- a) The command lines subfield of the ZAC lines, together with the start strobe line and the command strobe \$RRS, contain the control information necessary to execute the general cycles RGR and SGR. Each cycle is initiated by a start strobe; where successive start strobes shall not occur more frequently than specified in figures 2 and 4. When the Store Unit recognizes the assigned codes for the RGR or SGR command in the command lines, it shall not commence reading the address-specified core location and it shall not recognize any action with respect to the Command Strobe lines. As alternative action, the Store Unit shall transmit the existing contents of the Maintenance Register to, or load new contents into the Maintenance Register to/from the Data Lines.
- b) In order to determine if a register cycle is to be executed, the Storage Unit Controller shall continuously monitor the command field of the ZAC lines for the following command codes:

Command Lines	A	B	C	D	E
SGR =	1	0	1	1	1
RGR =	1	0	1	1	0

In addition, address bits A12 and A13 must both be set to the logical "one" state. All other address bits are ignored. The following equation specifies the functional intent, but is not intended to represent actual logic implementation:

$$A12 \cdot A13 \cdot (RGR + SGR) \cdot \$RRS = RGR \text{ or } SGR \text{ cycle executed.}$$

• If A12 and A13 are not both logical "ones," the memory will execute a Read/Restore (RRS) cycle (with no IA error reported) to the memory address specified by the address field.

- c) When transmitting RGR data to the System Controller, the Storage Unit shall be required to provide correct (odd) parity for both data words (bits 0-35 and bits 36-71).
- d) Information contained within the zone field of the ZAC lines shall be ignored for General Register cycles.
- e) Refer to para 2.5.7 of this specification and refer to the System Controller EPS-1 (43A219602) paragraphs 3.4.13, 3.4.13.6, 3.4.14, for further information on the useage of RGR and SGR commands.
- f) If a \$RRS is not received, an IA/Command Strobe Failure shall be reported, and the cycle aborted.
- g) If a \$CMD other than \$RRS is received (\$CW1, \$CW2, \$RCL), the Register Cycle shall be executed anyway just as if a \$RRS had been received.
- h) A parity error detected on ZAC information shall not cause a General Register cycle to be aborted, but an IA/ZAC parity error shall be reported by the Storage Unit.
- i) During an SGR command, a parity error detected on the incoming data (lines) shall not cause the SGR to be aborted, and the Maintenance Register (para 2.6.2) shall be set or reset according to the data received, and an IA/PU/PL (as appropriate) shall be reported by the Storage Unit.
- j) It should be noted that a store cycle with appropriate Command Strobe, where the command lines are transformed by fault to appear as requesting RGR or SGR, will be executed as the register cycle. Similarly, an intended register cycle, with command lines transformed by fault to appear as other than an RGR or SGR, will be executed as an aborted store cycle (see Section 1.4 and 4.1).

4.3

SIGNAL LINE CHARACTERISTICS

Standard Pulse Width	60 $\pm$ 20 ns (at 1.5 volts)
Transition Times	less than 10.0 ns (10% to 90%)
Logic Level "1"	4 $\pm$ 1 v. ("High" Voltage)
Logic Level "0"	0.3 $\pm$.3 v. ("Low" Voltage)

All statements of time in this specification are referenced at the Memory Port Board Free Edge connector and are measured at 1.5 volts potential. Figure 2 and figure 4 show when each signal is expected during the memory cycle.

FIGURE 4 A

SIGNAL WIDTH AND OCCURRENCE (HIGH SPEED STORE)

SIGNAL	WIDTH (ns)		OCCURRENCE (ns)	
	AVERAGE	TOLERANCE	AVERAGE	TOLERANCE
\$TS	60	$\pm$ 20	0	$\pm$ 0 by definition
ZAC	200	+120 Min. after \$TS	-30	+0 Max. -20 { Lines must be stable at "0".
\$CMD	60	$\pm$ 20	90	$\pm$ 30
\$ANS	70	$\pm$ 10	195	$\pm$ 10
\$XMIT-AP	60	$\pm$ 20	20	$\pm$ 20
DATA IN	100	$\pm$ 20	30	$\pm$ 20
\$XMIT-PA	120	$\pm$ 20	270	$\pm$ 10
DATA OUT	100	$\pm$ 20	340	Max.
IA	Next \$TS +110	$\pm$ 20	420	Max.
EOC	70	$\pm$ 10	220	$\pm$ 10

NOTE:

- (1) This table is a rigid specification of timing in the 655 Core Storage Unit.
- (2) \$CMD represents 4 lines; \$RRS or \$RCL or \$CW1 or \$CW2.
- (3) Time of "Occurrence" for high speed Storage Unit only.
- (4) If two Store Units are connected to one system controller, the leading edge of the \$ANS pulses must be within 20 nsec of each other in occurrence.

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4.3

SIGNAL LINE CHARACTERISTICS (continued)

FIGURE 4B

SIGNAL WIDTH AND OCCURRENCE (LOW SPEED STORE)

SIGNAL	WIDTH (ns)		OCCURRENCE (ns)	
	AVERAGE	TOLERANCE	AVERAGE	TOLERANCE
\$TS	60	± 20	0	± 0 by definition
ZAC	200	+120 Min. after \$TS	-30	+ 0 Max. Lines must - 20 be stable at "0".
\$CMD	60	± 20	90	± 30
\$ANS	70	± 10	850	± 20
\$XMIT-AP	60	± 20	20	± 20
DATA IN	100	± 20	30	± 20
\$XMIT-PA	120	± 20	940	± 10
DATA OUT	100	± 20	1015	Max.
IA	Next \$TS + 110	± 20	1095	Max.
EOC	70	± 10	910	± 20

NOTE: (1) This table is a rigid specification of timing in the 655 Core Storage Unit.

(2) \$CMD represents 4 lines; \$RRS or \$RCL or \$CW1 or \$CW2.

(3) Time of "Occurrence" for low speed Storage Unit only.

(4) If two Store Units are connected to one system controller, the leading edge of the \$ANS pulses must be within 20 nsec of each other in occurrence.

4.4 SIGNAL LINE DESCRIPTIONS4.4.1 START STROBE (\$TS)

Start Strobe shall be an inverted pulse, of standard pulse width, sent to the storage unit. It will start the storage unit timing, alert the storage unit to accept address, zone and command information, and shall reset the IA lines to the zero state.

4.4.2 ZONE LINES

There shall be 8 zone lines connected to the storage unit. The zone lines are to designate to the storage unit which portion(s) of an even or odd data word are to be altered during the execution of the Clear-Write by Zone storage unit command. The assignment of zone^{*} lines to bits in the even or odd data word is shown in Figure 3. If the least significant address bit (17) is a logical "0" the zone lines refer to the even data word. The zone lines have no effect for any cycle which is not a Clear-Write 1 cycle. For timing see Figures 2 and 4 (ZAC).

*NOTE: ---of para 2.5.3.1d.

4.4.3 ADDRESS LINES

There shall be 18 address transmission lines. The 2 high order Address Lines shall be ignored by the storage unit, except for the checking of parity. Address line "0" (A0) is the most significant address bit and address line "17" (A17) is the least significant address bit. For timing see Figures 2 and 4 (ZAC).

4.4.4 COMMAND LINES

There shall be 5 storage unit command lines. The logic levels of these lines represent a 5-bit operation code, which is part of the ZAC transmission. During normal store cycles, these command lines are functionally ignored (see Section 4.1). Only during general register cycles shall the command lines be used (see Section 4.2b). For timing see Figures 2 and 4 (ZAC).

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4.4.5 ZAC PARITY LINES

There shall be a ZAC parity line connected to the storage unit. It shall contain the (odd) parity information for the thirty-one (31) ZAC bits (8 Zone, 18 Address, and 5 Command bits). The Storage Unit shall check for correct ZAC parity on all Store Cycles and General Register cycles. For timing see Figures 2 and 4.

4.4.6 COMMAND STROBE LINES (Referred to as \$CMD)

The four command strobes are **negative** pulses of standard pulse width sent to the storage unit to specify the type of cycle to be executed. They are \$RRS, \$CW1, \$CW2, and \$RCL. Command Strobe lines are used for timing purposes only in the execution of RGR and SGR cycles (but only \$RRS is valid). For timing see Figures 2 and 4.

4.4.7 DATA LINES

There shall be 72 bi-directional data lines plus 4 unidirectional parity lines (2 from system controller, 2 to system controller). They shall be used to transmit or receive data.

4.4.8 INITIALIZE

Initialize is a level transmitted to the storage unit. The receipt of the initialize signal by the storage unit shall cause the logic to be placed in the preset or initial state with all the registers and faults cleared. The initialize signal shall not cause the contents of any memory location to be altered only if the memory is in the idle state. During the power-on sequence, the storage unit must initialize itself and not depend on the initialize signal.

The initialize signal shall be maintained valid for a minimum of 1 microsecond. The initialize line contains the complement of INZ. A high voltage level shall therefore represent no initialize signal, and a low voltage level shall represent an initialize signal.

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4.4.9 POWER FAIL

A "0" logic level is sent from the storage unit when the power supply has completed its power-on sequence. Whenever the power supply is operating within its specified margins the Power Fail line shall be a "0" logic level. When the power supply is shut down or in the power-on sequence, the Power Fail line shall be a "1" logic level or floating. Floating is defined as that state where the line receiver cannot draw more than 1 milli-amp of current.

The Power Fail line shall indicate a power shut-down warning to the external device (System Controller) by providing the logical "1" level 50 microseconds prior to actual shut-down.

4.4.10 TEMPERATURE WARNING

A "0" logic level is sent from the core stack when the temperature of the stack is within its operating margins. When the temperature has exceeded these margins, the line shall be a "1" logic level or floating. It shall light the overtemperature indicator and turn on a local audible alarm (see Section 3.1.6). This line shall not be sent to the system controller.

4.4.11 ANSWER LINE (\$ANS)

The Answer Pulse shall acknowledge to the system controller that a cycle has been started. For timing see Figures 2 and 4.

4.4.12 END OF CYCLE LINE

The Storage Unit End of Cycle pulse is transmitted to the System Controller for "look ahead" purposes. The EOC pulse indicates that the storage cycle requested will be completed within a prescribed time. Refer to figures 2 and 4 for timing details.

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4.4.13

ILLEGAL ACTION LINES

The illegal action lines indicate parity and timing error status to the system controller. IA codes 1 through 3 are not applicable to the execution of the RGR and SGR commands. For timing see Figure 5.

When more than one illegal action occurs simultaneously, only the code with the highest priority is transmitted. The priority is shown in the table; the lowest (priority) number shown has the highest priority.

These lines are coded as follows:

IA# (Octal)	PRIORITY	ILLEGAL ACTION LINES				
		IA ₀	IA ₁	IA ₂	IA ₃	
0	4	0	0	0	0	No illegal actions
1	3	0	0	0	1	Read parity error PL
2	3	0	0	1	0	Read parity error PU
3	3	0	0	1	1	IA #1 and IA #2*
4	1	0	1	0	0	Command Strobe time out
5	2	0	1	0	1	Write parity error PL
6	2	0	1	1	0	Write parity error PU
7	2	0	1	1	1	IA #5 and IA #6
10	None	1	0	0	0	Unused
11	None	1	0	0	1	Unused INVALID
12	None	1	0	1	0	Unused
13	None	1	0	1	1	Unused
14	2	1	1	0	0	ZAC parity error
15	2	1	1	0	1	IA #14 and IA #5
16	2	1	1	1	0	IA #14 and IA #6
17	2	1	1	1	1	IA #14 and IA #7

*See Table 3.3 of 43A219602 (System Controller).

4.4.13.1

READ PARITY PL

IA Code 1

Read Parity Error PL status is returned to the system controller when a parity error has been detected in data bits (36-71) as read from core. Normally, the command is not aborted (see para 2.6.3).

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4.4.13.2 READ PARITY ERROR PU

IA Code 2:

Read Parity Error PU status is returned to the system controller when a parity error has been detected in data bits (0-35) as read from core. Normally, the command is not aborted (see para 2.6.3).

4.4.13.3 COMMAND STROBE FAILURE

IA Code 4:

Command Strobe Failure status is returned to the system controller when the Command Strobe does not follow the start strobe within a specified time (see figures 2 and 4); or multiple command strobe lines are logical ones*during the memory operations RRS, RCL, CW1, CW2. The command is aborted. The preceding is applicable to RGR and SGR cycles also.

*Note: Not a requirement of initial storage units.

4.4.13.4 WRITE PARITY ERROR PL (CW1 and CW2 ONLY)

IA Code 5:

Write Parity Error PL status is returned to the system controller when a parity error has been detected on the incoming Data Lines 36-71. Normally, a CW2 command is aborted (but see para 4.4.14). A CW1 is aborted if address bit 17=1.

4.4.13.5 WRITE PARITY ERROR PU (CW1 and CW2 ONLY)

IA Code 6:

Write Parity Error PU status is returned to the system controller when a parity error has been detected on the incoming Data Lines 0-35. Normally, a CW2 command is aborted (but see para 4.4.14). A CW1 command is aborted if address bit 17=0.

4.4.13.6 ZAC PARITY ERROR

IA Code 14:

ZAC Parity Error status is returned to the system controller when a parity error has been detected on ZAC lines; or if the zone field is zero for a CW1 command.* The command is aborted.

*Note; See para. 2.5.3.3.

4.4.14 OVERRIDE PARITY LINE

The override parity line signal from the System Controller allows the Storage Unit to store the data in memory as received on the data lines. This signal from the system controller allows storage operation with even data parity only during a CW2 operation (para 2.5.4) without an abort occurring.

However, when a data parity error is detected by the storage unit, an Illegal Action shall be reported to the System Controller.

This line must be stable throughout the memory cycle. If the storage unit detects a ZAC parity error, the command shall be aborted.

4.4.15 TRANSMIT PULSE (\$XMIT)

The \$XMIT Pulse is used to strobe data into receive register. A \$XMIT-AP strobes data into the receive register of the core store. The \$XMIT-PA strobes data into the receive register of the system controller. For timing see Figures 2 and 4. These are positive going pulses.

5.0 GENERAL DESIGN REQUIREMENTS

The MQX Core Storage Unit shall conform to the EPS: General Design Requirements for GE-655 and GE-355 Systems 43A177851.

5.1 AC POWER

Although this unit is defined as a Central System Module, it shall be designed to function with the AC power specifications defined by para 4.1.3 of 43A177851. (AC power for peripherals) with the added requirement to operate down to 50 Hertz* (at specified AC voltage) for a period of 10 seconds (to utilize the Motor Generator ride through capability).

*Note: Desirable but not mandatory on initial Storage Units; required on subsequent models of the Storage Unit.

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6.0 RELIABILITY AND MAINTAINABILITY

As a maintainability aid, the 655 Core Storage Unit shall use partitioned logic boards compliant with the organization requirements as specified in the MQX Board Tester EPS-1 - 43A177854 and the MQX Board Tester Design Memos (1-6).

6.1 MAINTENANCE OBJECTIVES

6.1.1 Scheduled Preventative Maintenance

The amount of scheduled preventative maintenance for the core storage unit should be no more than 15 minutes for every 200 hours of machine power on. Maintenance will include an air filter check and a T&D run under high and low margin conditions.

6.1.2 Unscheduled Maintenance

The mean time to repair (MTTR) shall be in accordance with the standards set by the 655 Maintainability Design EPS - 43A219617.

6.1.3 Maintenance Cost

The annual maintenance cost for the core storage unit shall not exceed two percent of shop cost. This cost includes material and labor for both scheduled and unscheduled maintenance.

6.1.4 Diagnostic Programs

To aid in factory testing and to provide a tool for field engineering, diagnostic programs will be provided by engineering prior to the first production test cycle. Hardware features will be included to aid diagnostic programming.

6.1.5 Maintenance Features

Store system core stack failures are predominantly interconnections and as core stack assemblies are not normally spared at each computer site, available data on 600 line system down time due to memory stack failure indicates MTTR's of hours to a day or more. Therefore, a strong effort shall be made to reduce the effect of core stack failures. Such effort shall take the form of spare bits added to each basic stack module. The spare bits shall include wired cores and drive and sense circuits. The method of disconnect from a detected bad bit and interconnect to a spare bit shall be simple yet not degrade performance of the core storage unit. Three spare bits shall be provided for each 36-bit word.

6.2 RELIABILITY6.2.1 AVAILABILITY

The subsystem availability objective shall be a minimum of 99 percent where:

$$\text{AVAILABILITY} = \frac{\text{MTBF}}{\text{MTBF} + \text{MTTR}} \times 100$$

or

$$\text{MTBF} \geq 99 \text{ MTTR.}$$

6.2.2 EQUIPMENT LIFE

The equipment shall have a normal service life of not less than 10 years, with only normal maintenance performed at the computer installation.

6.2.3 MEAN TIME BETWEEN FAILURE

The minimum acceptable MTBF shall be in accordance with the standards set by the GE-655 Maintainability Design EPS-43A219617.

6.2.4 ERROR RATE

The storage unit with 64K 36-bit words shall have a non-recoverable error rate not to exceed 1 in 10^{14} bits.

6.2.5 TRANSIENT ERROR RATES

A transient error is defined as a momentary error. It may not be repeated in the sense that it can be made to recur but it is not a hard or continuous error as might be caused by a hard component, wire run, etc., failure.

The criteria for measuring transient error rates shall be the signal to noise ratio as seen on the internal cabinet wiring. The mean signal to noise ratio for the 655 Storage Unit shall be 8.5 or greater at a 90% confidence level. No sampled ratio shall be less than 8.0 Signal to noise ratio as used here is the voltage threshold level for going from a "0" to a "1" divided by the RMS value of the noise voltage.

6.2.6

MEASUREMENT OF TRANSIENT ERROR RATE

This paragraph does not define explicitly how the transient error rate or signal to noise ratio should be measured, but it does point out some of the things that need to be considered in making this measurement.

The selection of points in a cabinet to be measured should take into account which signals are critical in the sense that false momentary triggering will cause an error. In addition, the location and/or bunching of such signals should be considered. That is to say, sample points should be selected from both densely and sparsely populated areas.

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6.2.6 Measurement of Transient Error Rate (continued)

In determining the size of the sample to be taken, it should be acceptable to assume that the standard deviation of the sample and the entire population are equal and that the distribution of the means of all possible samples is normal. This then implies the following:

$$\frac{\sum_{i=1}^n (S/N)_i}{n} + \frac{1.28 \sigma_s}{\sqrt{n}} \leq (S/N)_{\text{spec}}$$

where: $(S/N)_i$ = Signal to noise ratio of the i^{th} sample

n = Sample size -- greater than 30

σ_s = Standard deviation of the sample

$$\sigma_s = \left(\frac{\sum_{i=1}^n (S/N)_i^2 - \frac{1}{n} \left(\sum_{i=1}^n (S/N)_i \right)^2}{n-1} \right)^{\frac{1}{2}}$$

$(S/N)_{\text{spec}}$ = Specified signal to noise ratio.

Averaging of signal to noise ratios in this manner to gain some assurance of a cabinet transient error rate is not theoretically sound unless the spread on the ratio is small. For this reason the minimum value of 8.0 has been selected.

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